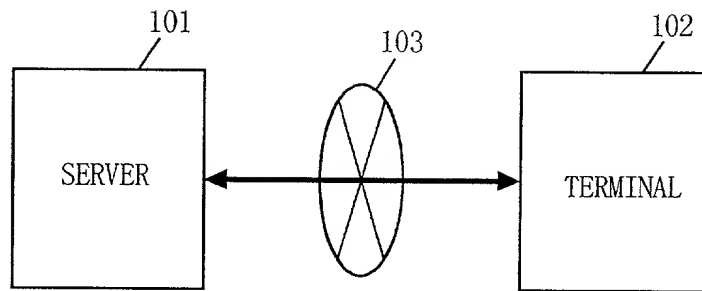


F I G. 1



F I G. 2

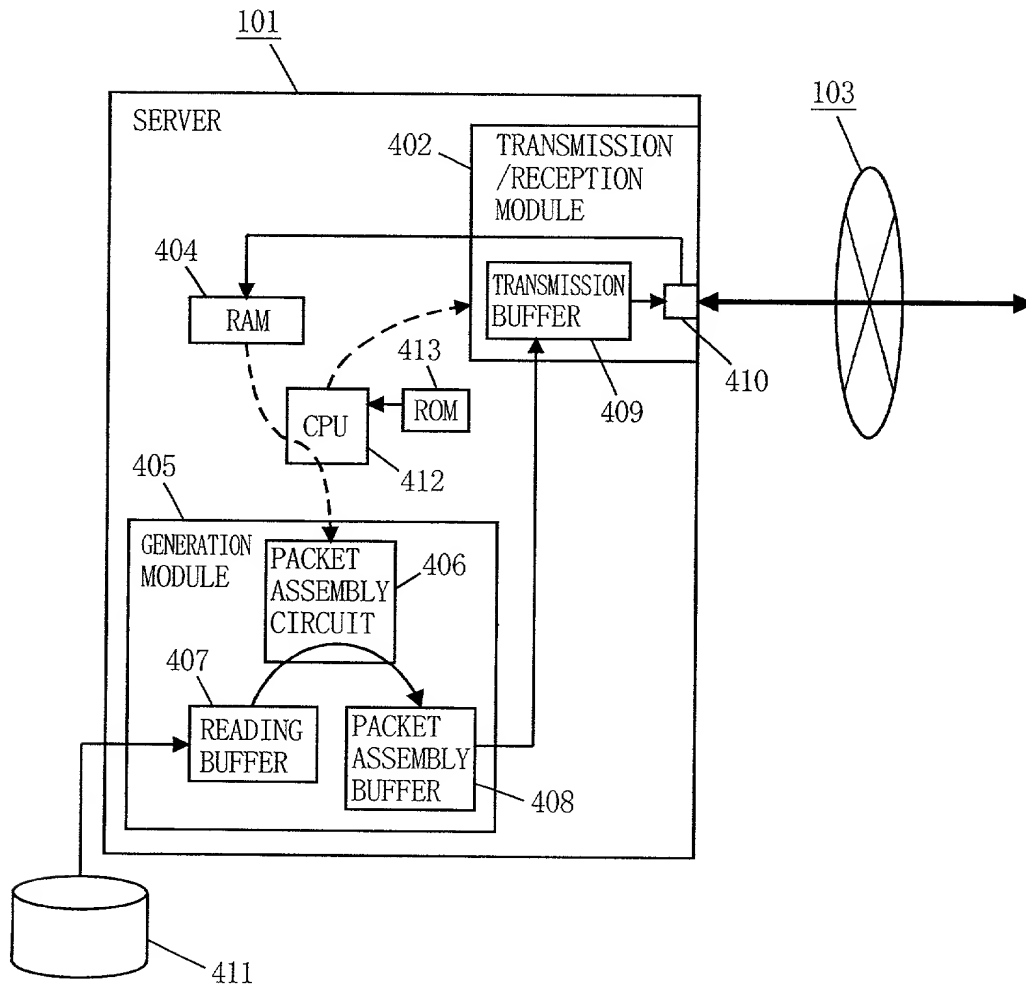


FIG. 3

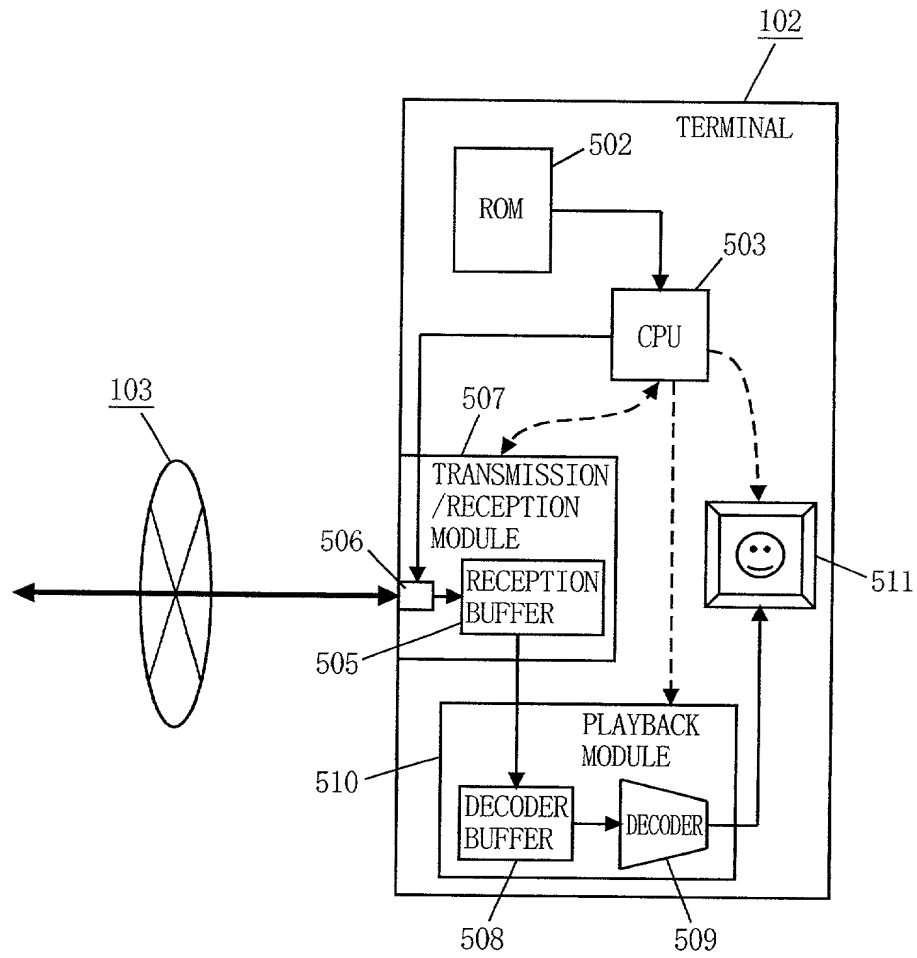


FIG. 4

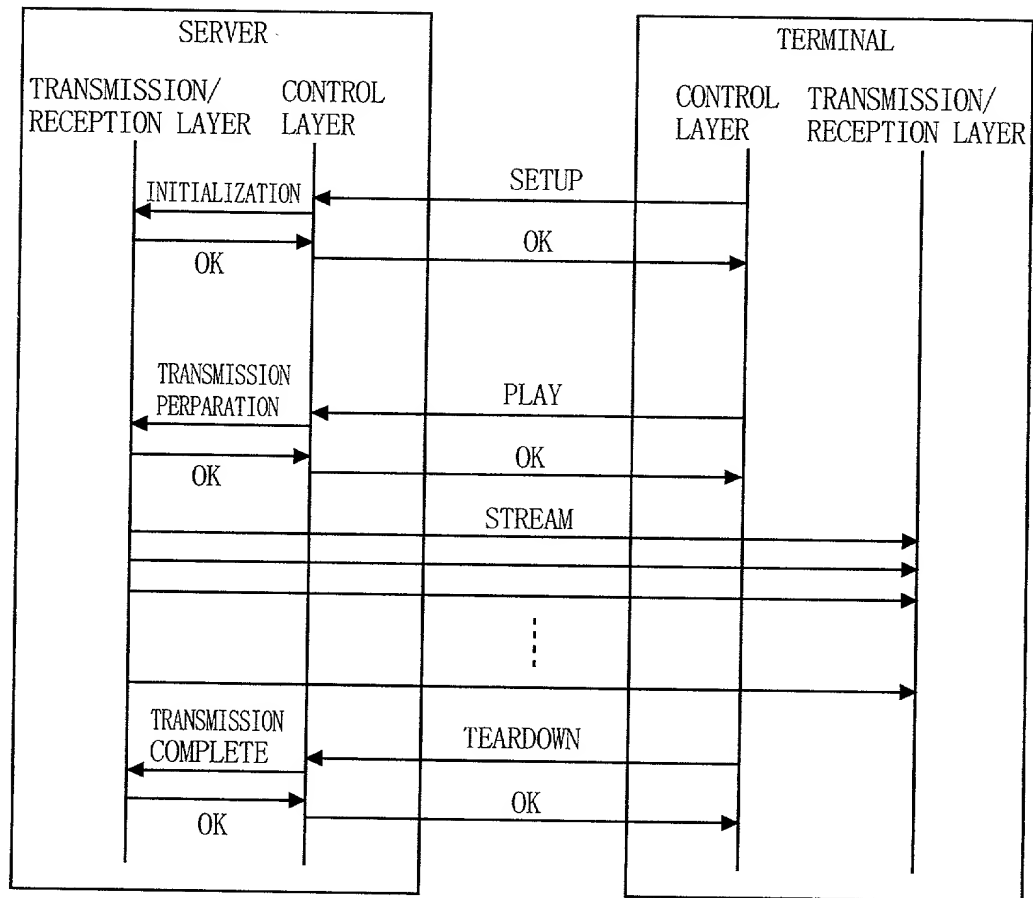


FIG. 5

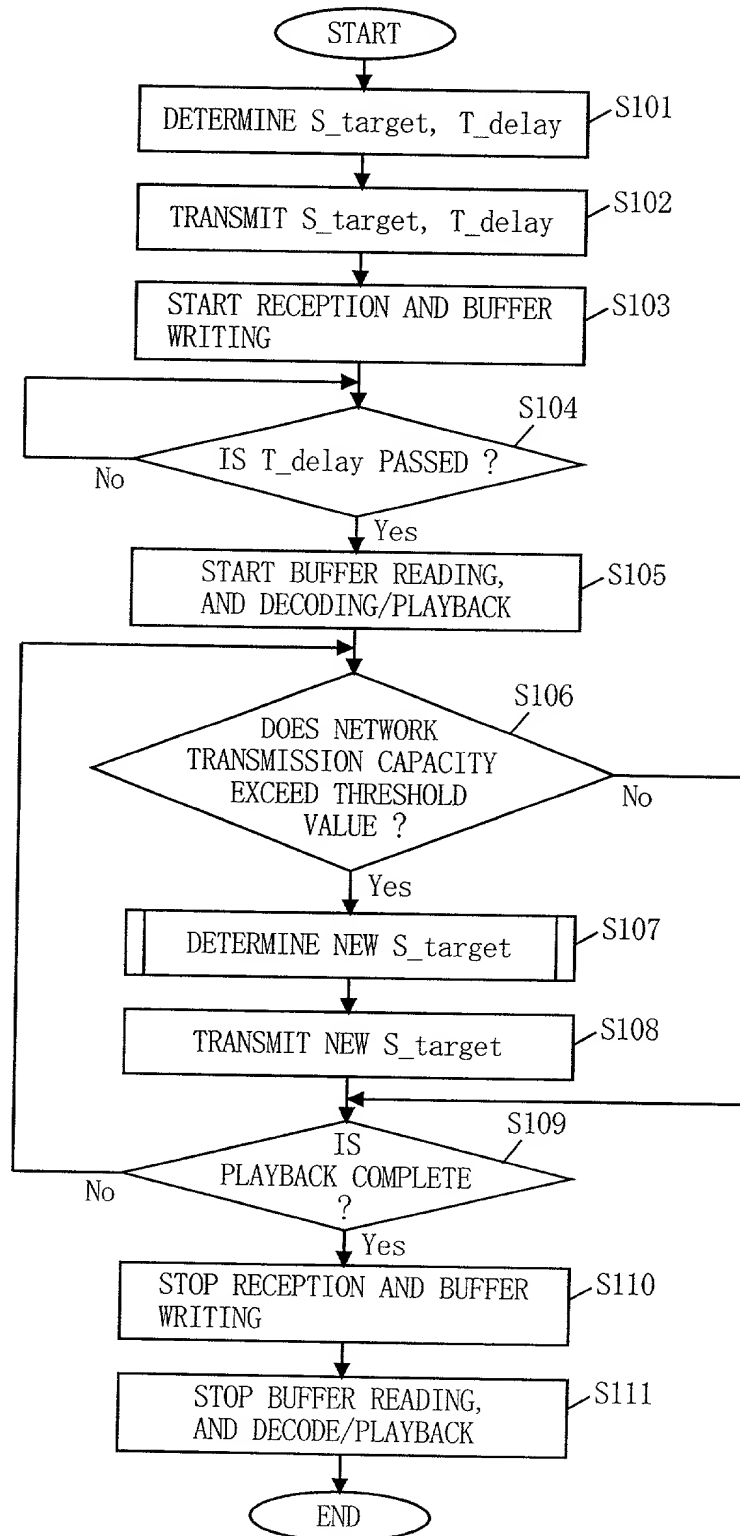


FIG. 6

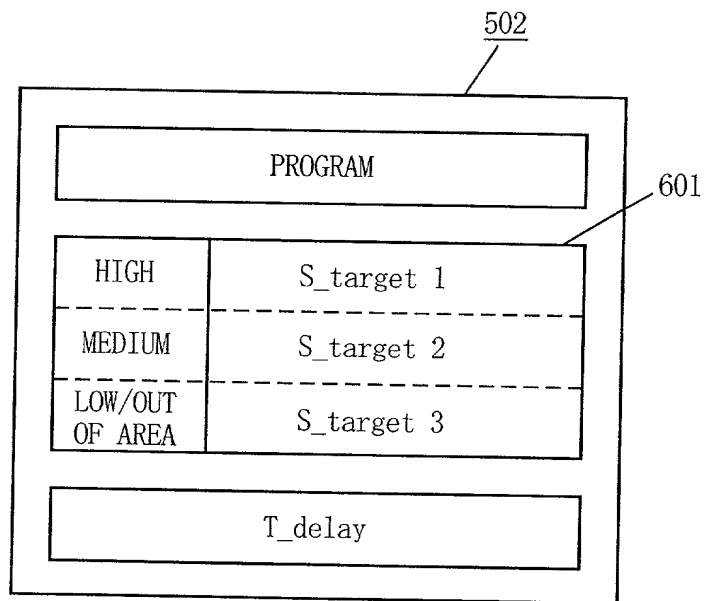


FIG. 7A

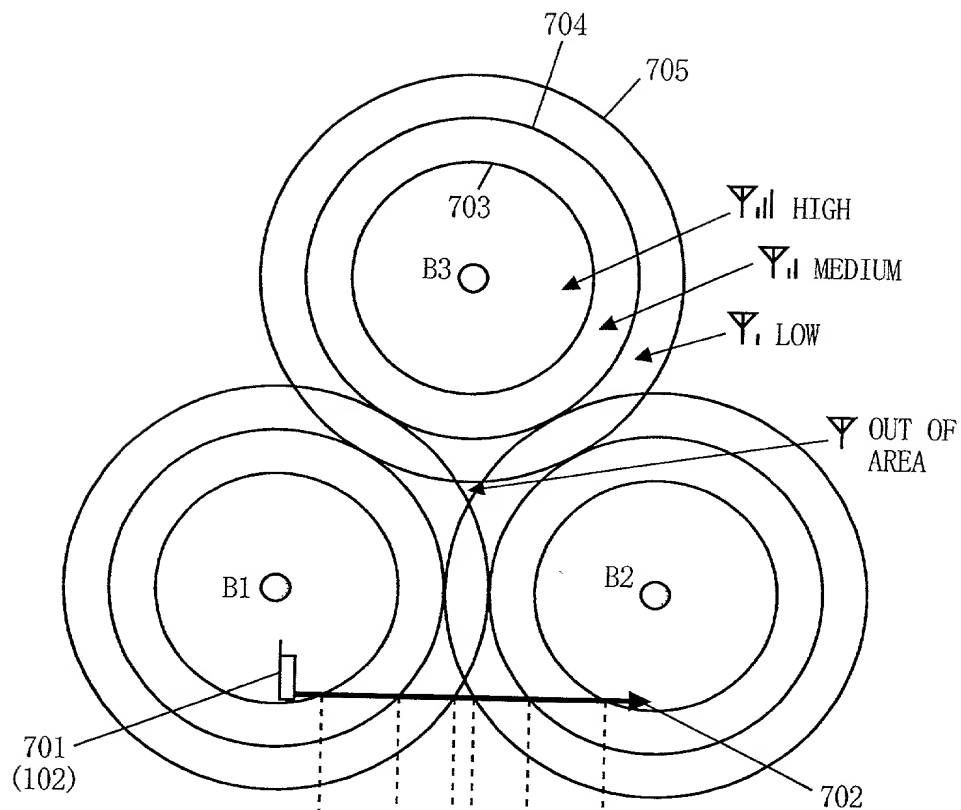


FIG. 7B

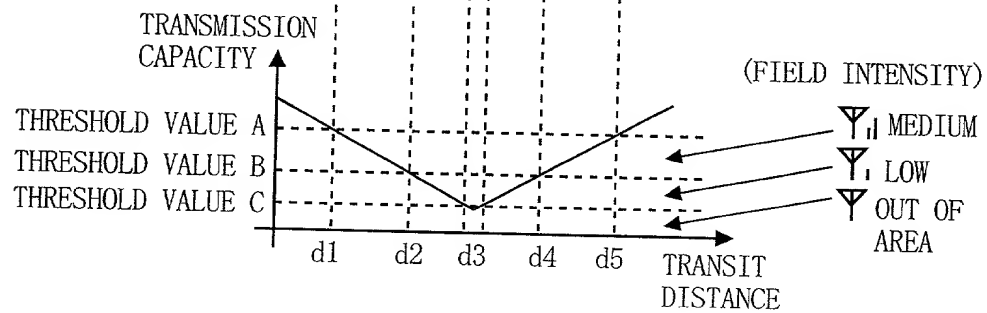


FIG. 8

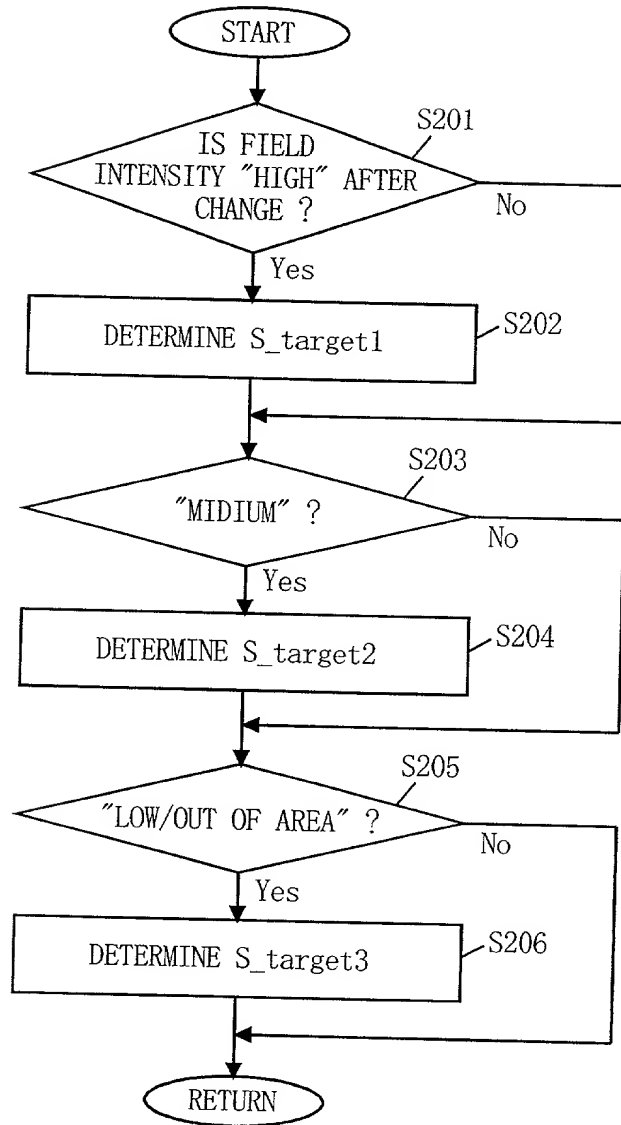


FIG. 9

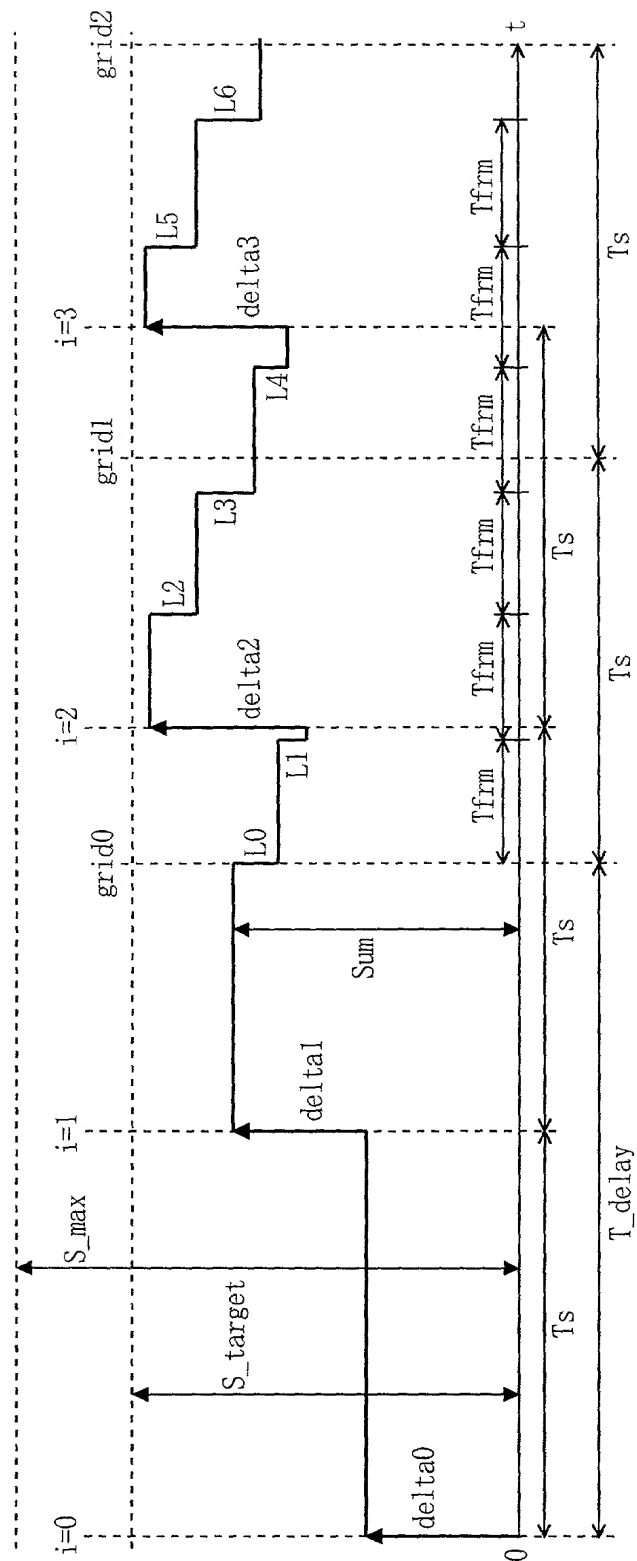


FIG. 10

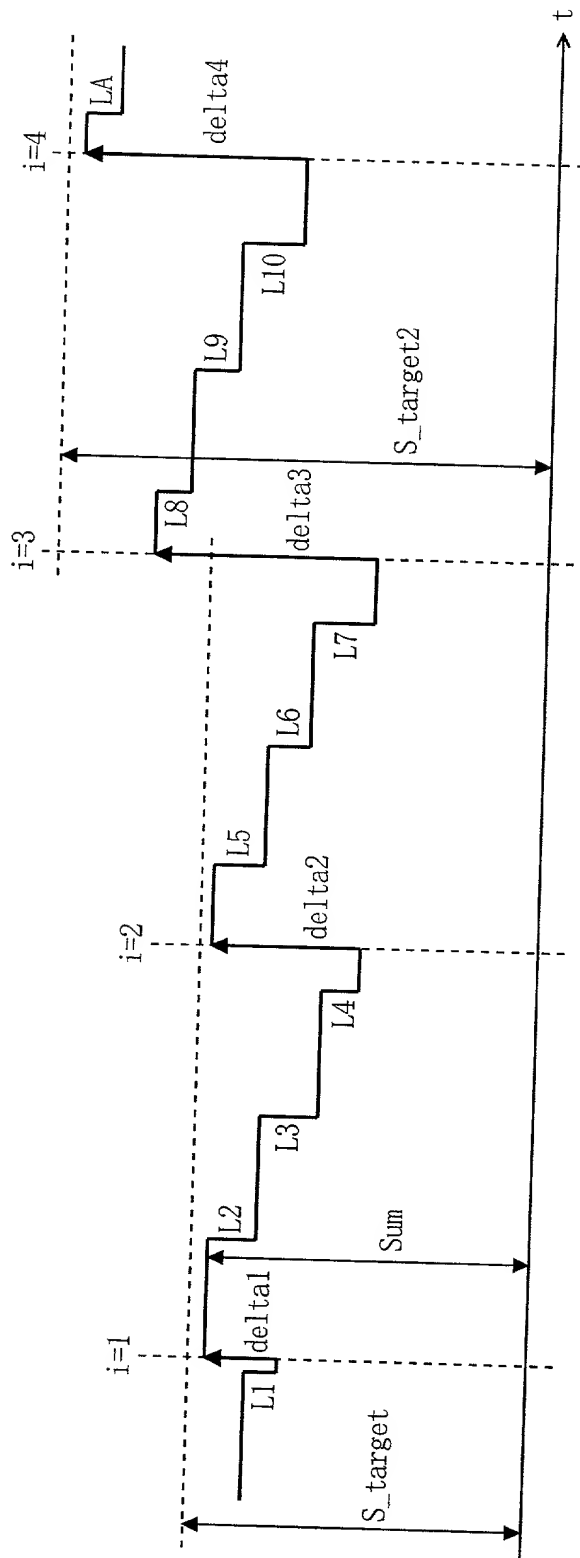


FIG. 11

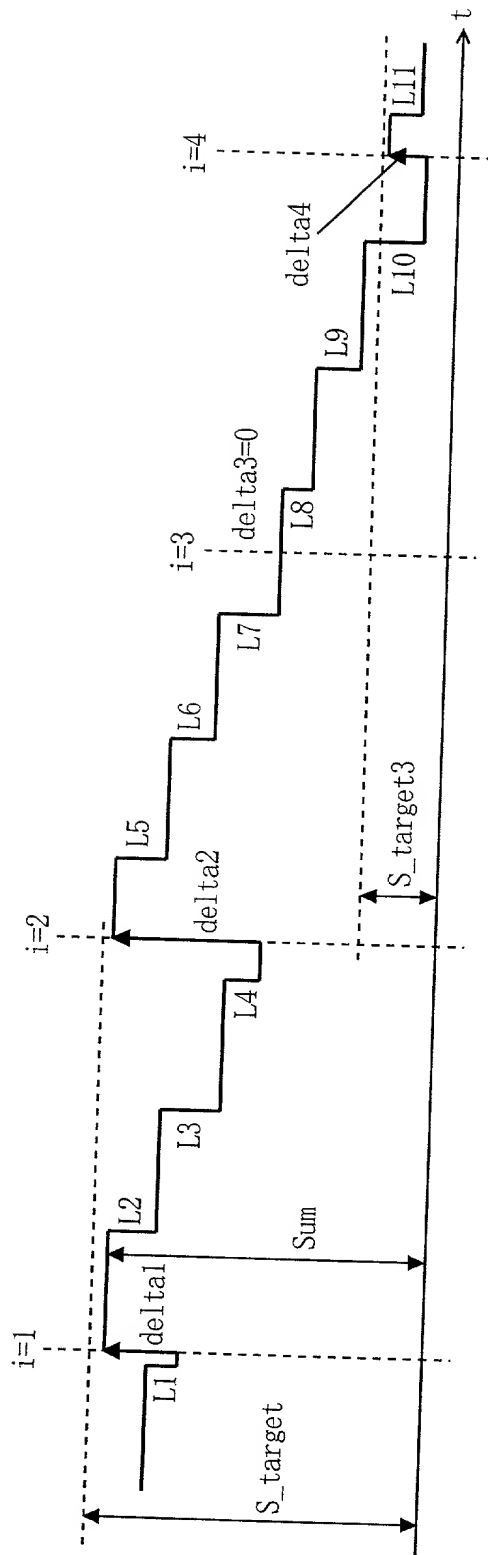


FIG. 12

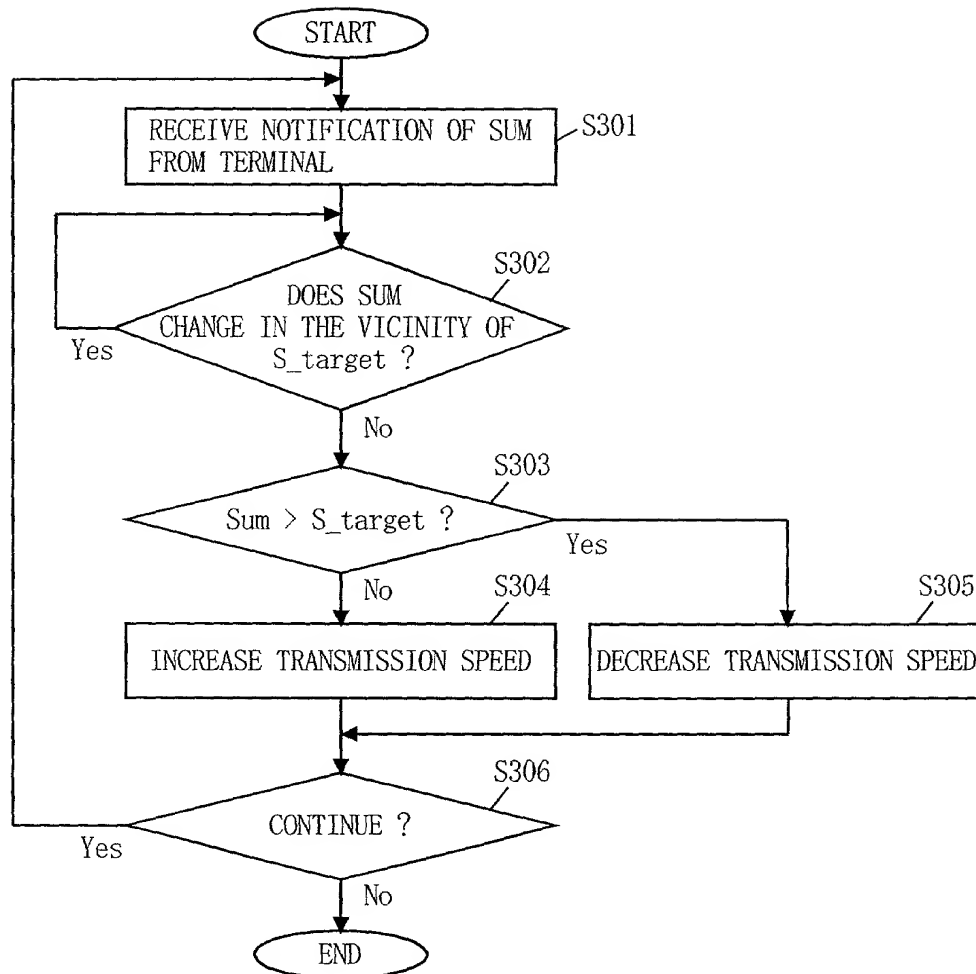


FIG. 13

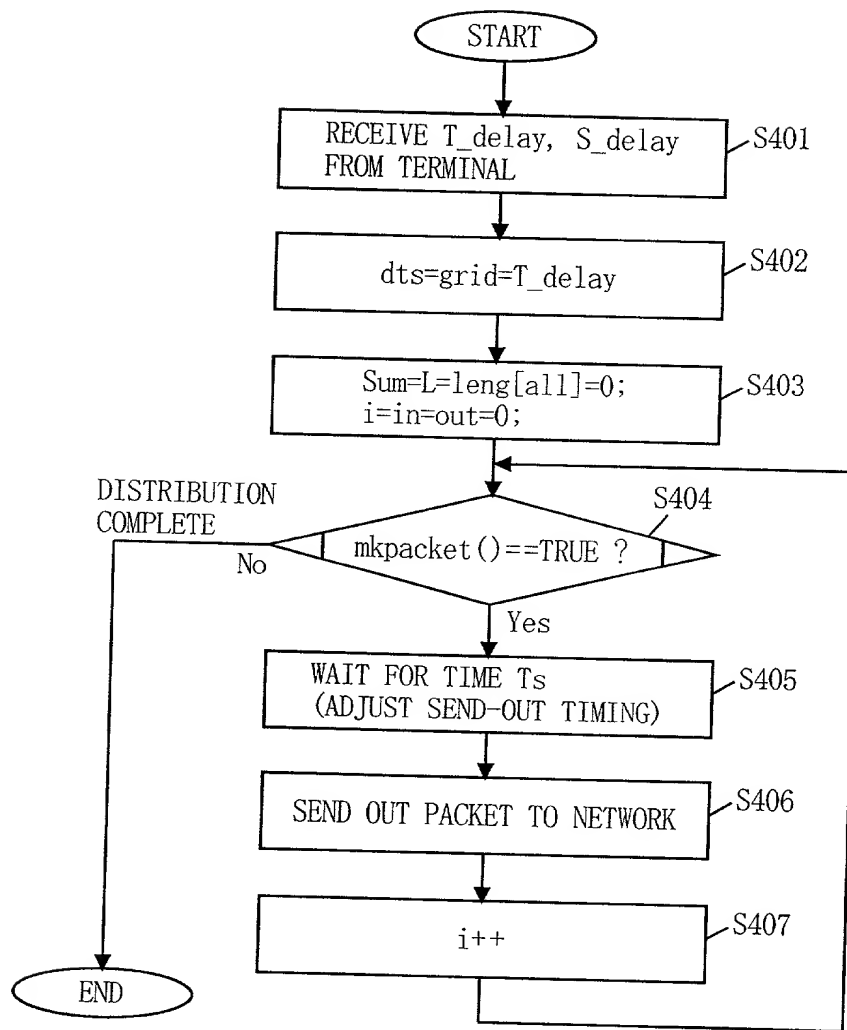
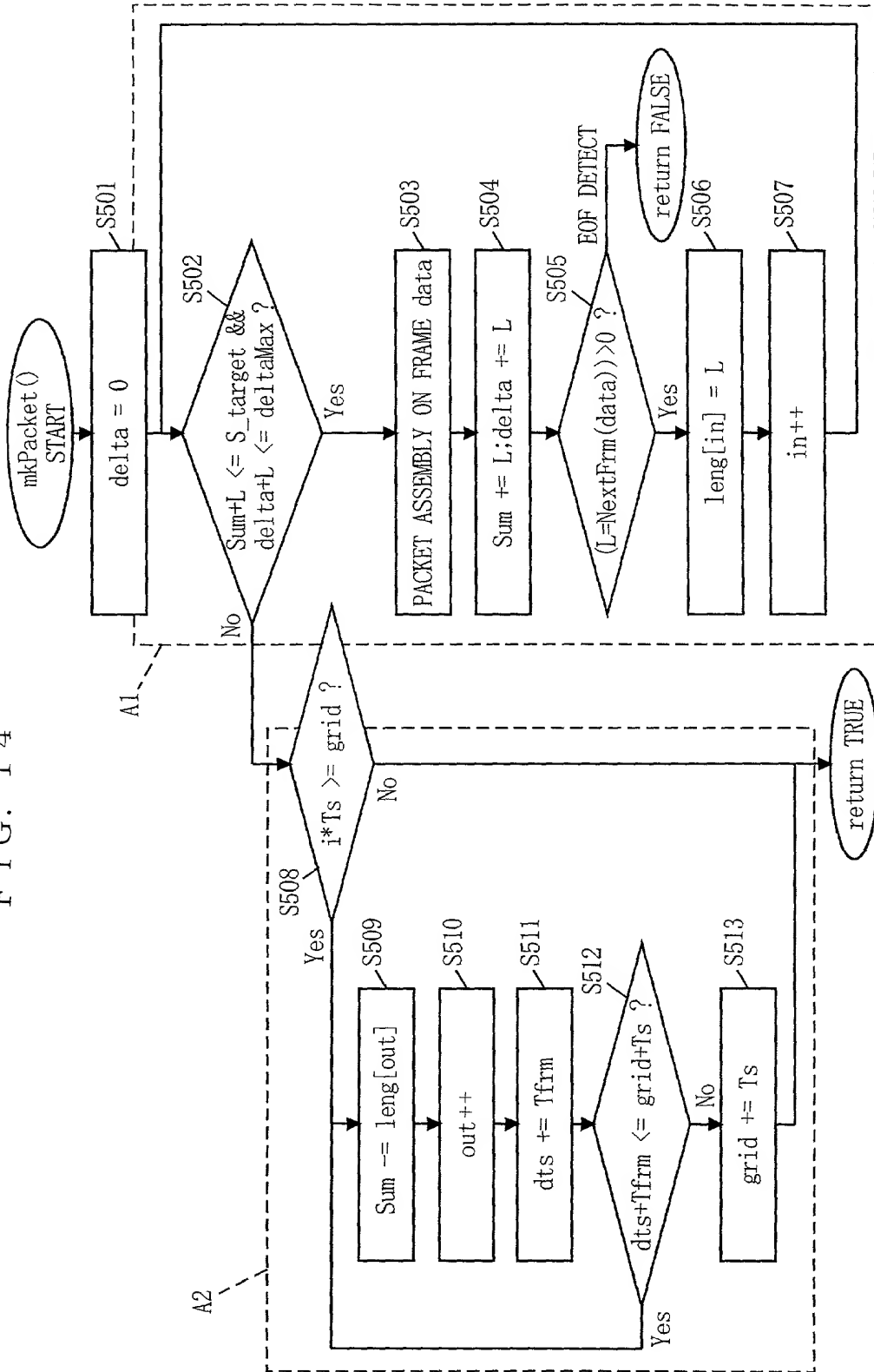
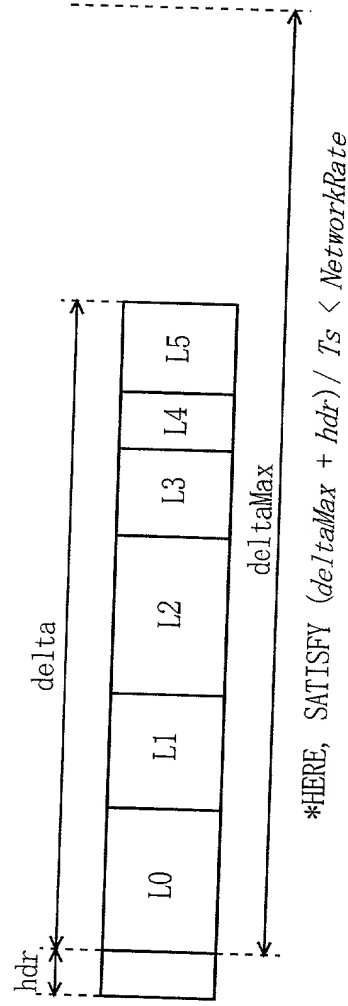


FIG. 14



(A) of FIG. 15



(B) of FIG. 15

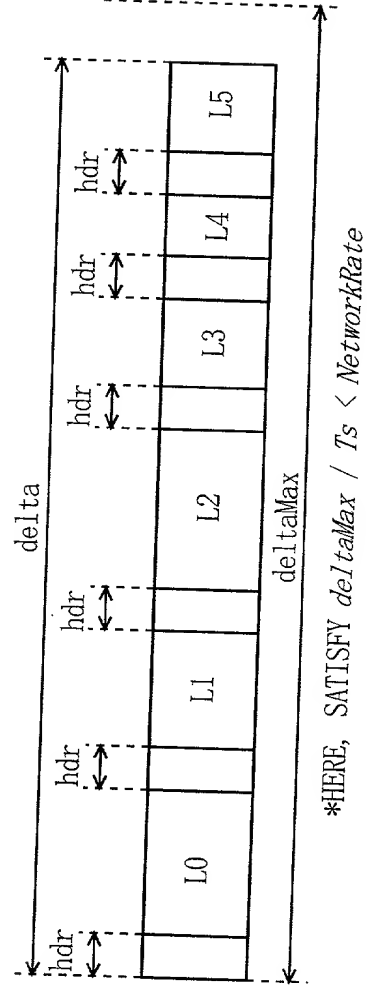


FIG. 16

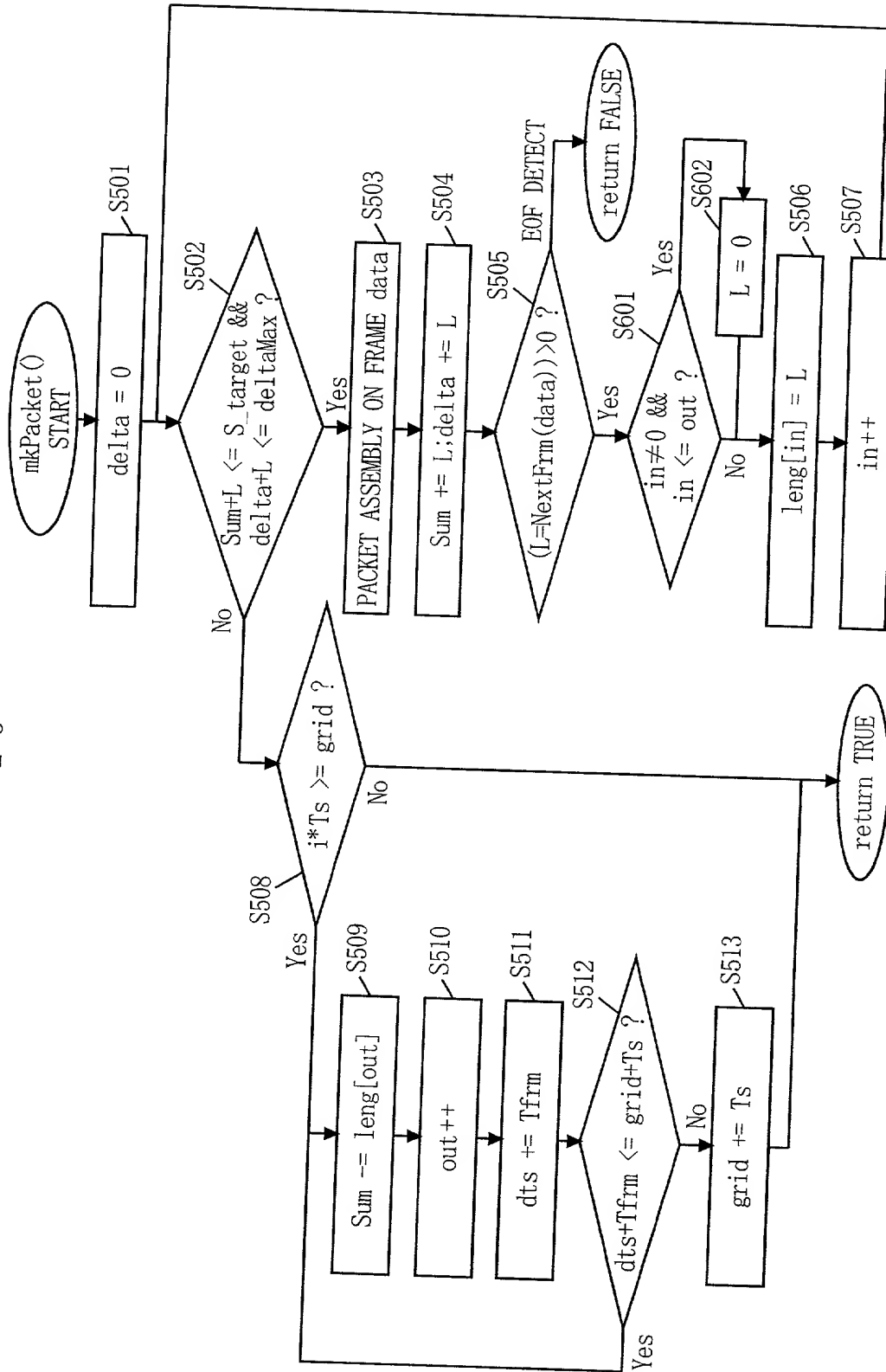


FIG. 17

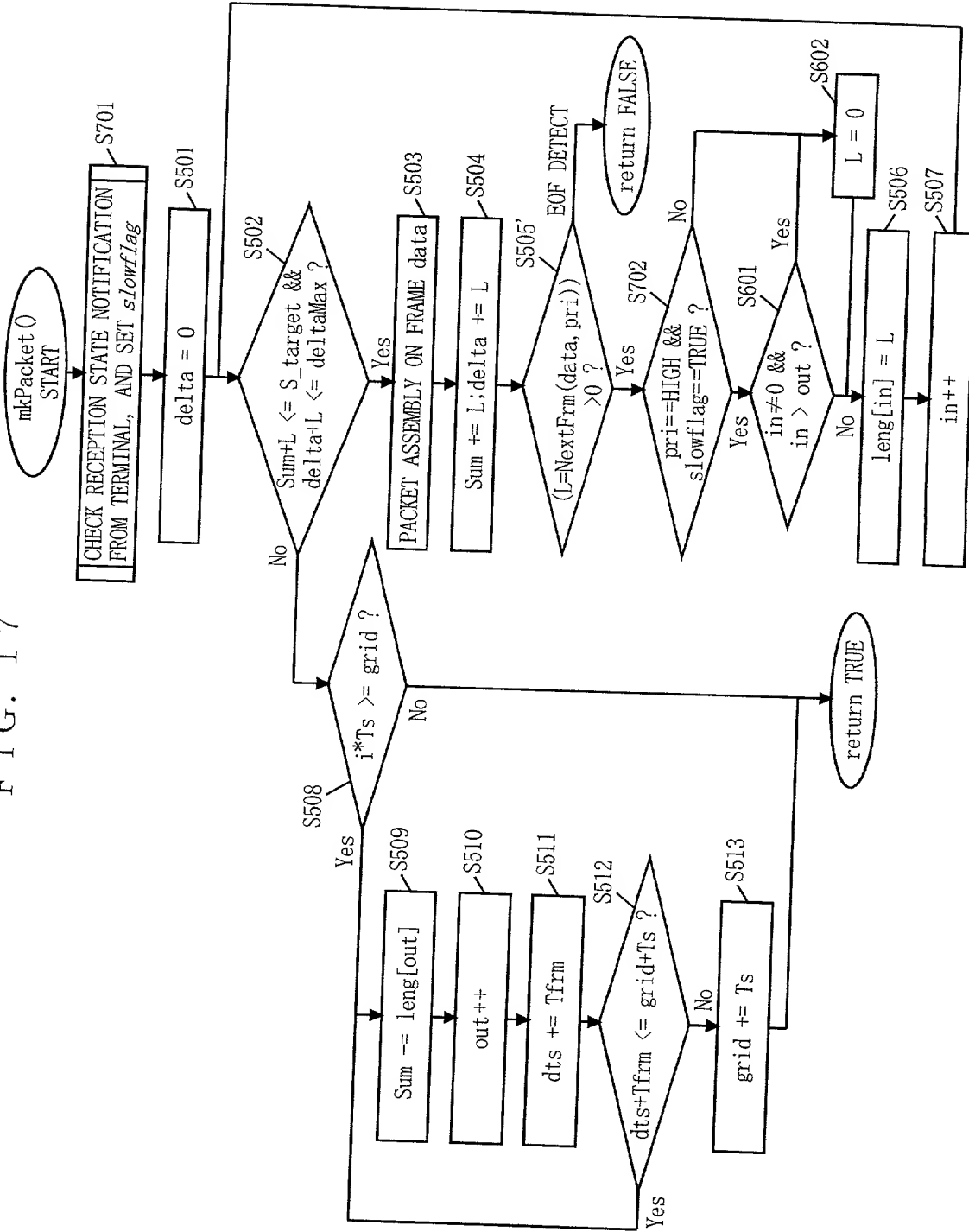
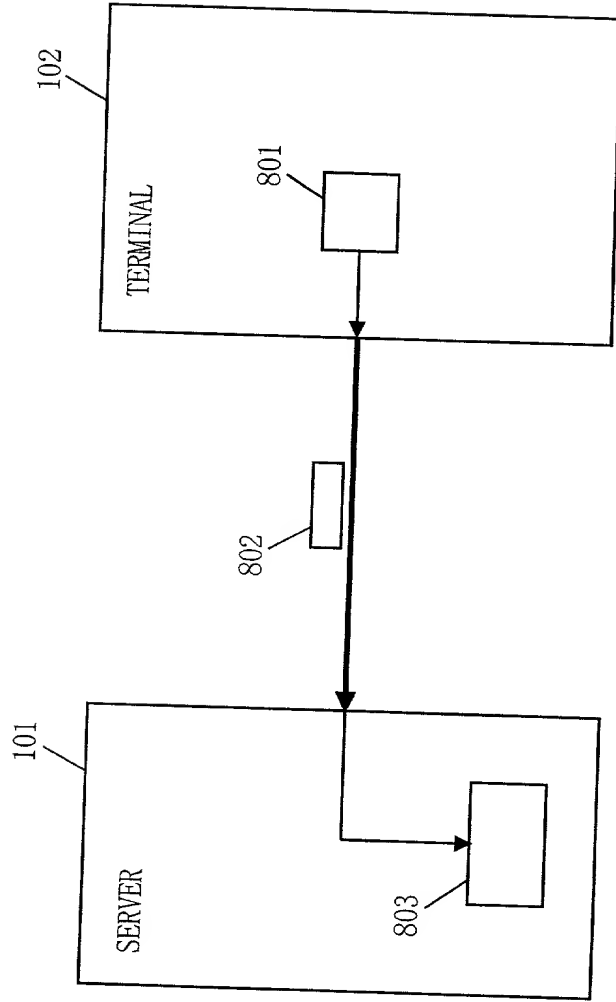
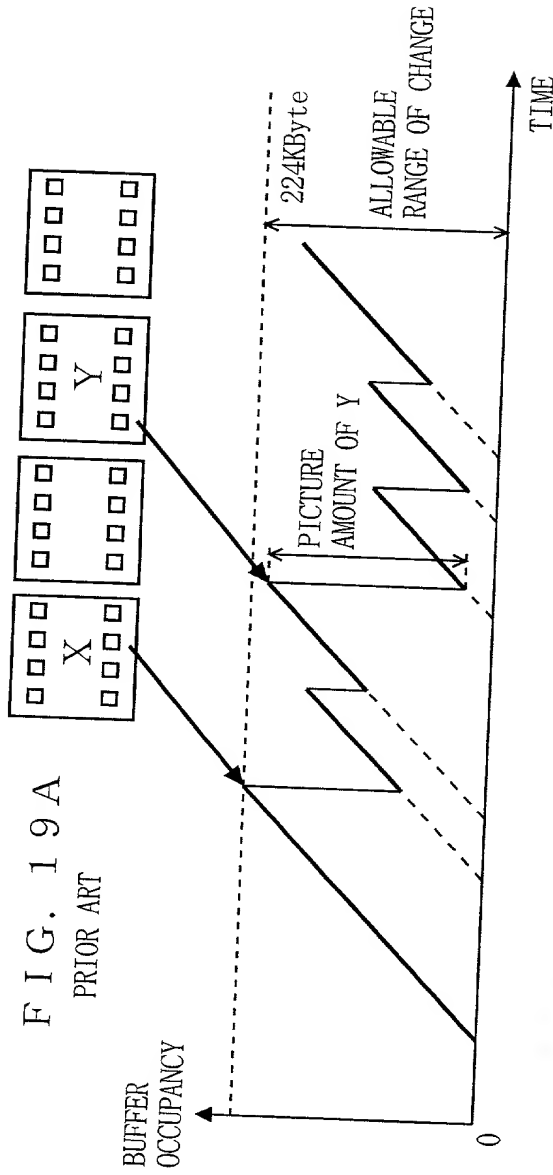


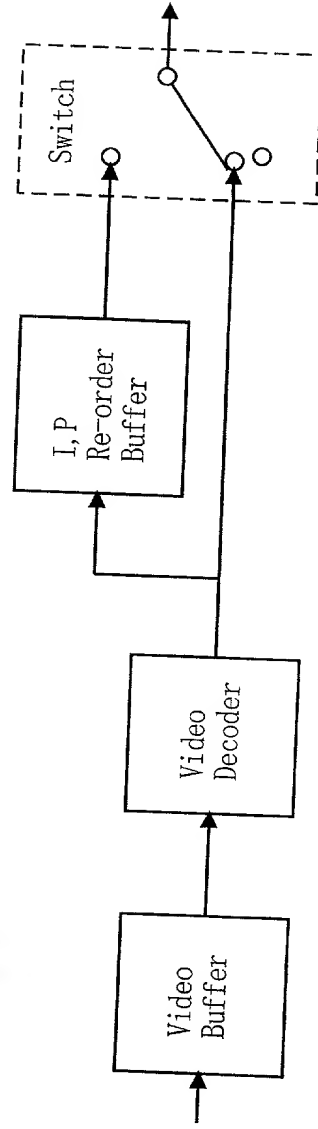
FIG. 18 is a block diagram of a system architecture. The system includes a SERVER (101) and a TERMINAL (102). The SERVER (101) contains a component 803. The TERMINAL (102) contains a component 801. A communication line (802) connects the SERVER (101) and the TERMINAL (102). Arrows indicate data flow from the TERMINAL (102) to the SERVER (101) and from the SERVER (101) to the component 803.

FIG. 18





vbv_delay



F I G. 2 0 P R I O R A R T

